ABSTRACT OF THE DISCLOSURE

Logic synthesis is conducted for CP apertures 44 using standard cells corresponding to shaping holes 4 used in logic design of a system and placed at first placement positions on the respective CP apertures 44. A CP aperture 44 used for exposure is selected from among the CP apertures for which logic synthesis has been conducted. Second placement positions of the standard cells on a substrate which standard cells correspond to the shaping holes 4 provided on the selected CP aperture 44 and wiring routes among the standard cells are calculated.